Electronic Version
Stylesheet Version v1.1.1

[TRANSPARENT LATCH CIRCUIT]

Abstract

The present invention provides a transparent latch circuit capable of performing a scan test in general scan design (GSD). In the transparent latch circuit a test signal is at a Low level during normal operation. Since a latch stop circuit outputs a High-level latch stop signal, a slave latch circuit has a received signal pass through it directly and a master latch circuit operates as a latch circuit in response to a signal output from an inverter. On the other hand, a test signal is at a High level during scan test. At this point, the latch stop circuit outputs a signal complementary to the signal output from the inverter. Therefore, the master latch circuit and the slave latch circuit operate as latch circuits responding to signals complementary to each other. Thereby, the entire transparent latch circuit operates as a flip-flop circuit.